



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,122	06/12/2002	Chien-Hung Liu	MXIP0043USA	1153

27765 7590 04-15-2003

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)  
P.O. BOX 506  
MERRIFIELD, VA 22116

EXAMINER

HUYNH, ANDY

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 04/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/064,122

Applicant(s)

LIU ET AL.

Examiner

Andy Huynh

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 12 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 June 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other \_\_\_\_\_

Art Unit: 2818

## DETAILED ACTION

### *Acknowledgment*

1. Claims 1-20 are pending in the application is acknowledged.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims **1-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Lai et al. (USP: 6,432,778 B1, hereinafter "Lai").

Regarding claims **1-2, 4, 12, and 14**, Lai discloses in Fig. 12 a system on chip (SOC) 100 characterized by nitride read only memory (NROM) 142 and read only memory (ROM) 144, 146, the system comprising:

a P type silicon substrate 102 of a first conductivity type P, a nitride read only memory (NROM) area 105, a read only memory area 106 and a periphery area 103 defined on a surface of the substrate;

a plurality of ONO (oxide-nitride-oxide) layers 118 disposed along a first direction in the nitride read only memory area and the read only memory area, a conductive doping area 122 with a second conductive type N positioned in the substrate between each ONO layer and used as bit lines of the system on chip;

Art Unit: 2818

an oxide layer 128 positioned atop each bit line:

a plurality of word lines 134 covering each ONO layer in the nitride read only memory area and the read only memory area, the word lines disposed along a second direction and forming a nitride read only memory cell at the intersection of each ONO layer in the nitride read only memory area, and a read only memory cell 146 at the intersection of each ONO layer in the read only memory area;

a plurality of doping areas, each doping area optionally positioned in the substrate at a bottom of a read only memory cell to cause the read only memory cell with the doping area and a read only memory without the doping area to have at least two different threshold voltages low  $V_{th}$  and high  $V_{th}$ , respectively, to present two different storage states "0/1" ;

a plurality of periphery circuit devices 136 positioned on the substrate in the periphery area;

at least one inter-layer dielectric (ILD) and at least one pattern metal interconnect layer subsequently covering the nitride read only memory area, the read only memory area and the periphery area; and

a plurality of plugs positioned in the inter-layer dielectric for electrically connecting each device positioned in the nitride read only memory area, the read only memory area and the periphery area through the metal interconnect layer (column 4, line 7-column 7, line 3).

Regarding claims **3 and 13**, Lai discloses in Fig. 12 two pocket ion implantation areas of the first conductive type are disposed in the substrate at two sides of each bit line.

Regarding claims **5-6 and 15-16**, Lai discloses a thickness of the ONO layers ranges from 100 to 250 angstroms; the ONO layer is formed a stacked structure comprising a bottom

Art Unit: 2818

oxide layer 112 with a thickness ranging from 20 to 150 angstroms, a silicon nitride layer 114 with a thickness ranging from 20 to 150 angstroms, and a top oxide layer 116 with a thickness ranging from 50 to 150 angstroms (column 4, lines 43-62).

Regarding claims **7-8 and 17-18**, Lai discloses each word line is composed of a polysilicon layer; a polysilicide layer is formed on a surface of the polysilicon layer (column 6, lines 18-22).

Regarding claims **9 and 19**, Lai discloses the read only memory is a mask read only memory (mask ROM, MROM) (column 10, claim 15).

Regarding claims **10 and 20**, Lai discloses the plurality of doping areas are formed by utilizing an ion implantation process capable of optionally implanting ions into the substrate at a bottom of a read only memory cell to form ROM code (column 6, lines 41-56).

### *Conclusion*

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Chang et al. (USP: 6,461,949 B1), Lai et al. (USP: 6,448,126 B1), Boaz (USP: 6,297,096 B1), Abeln et al. (USP: 6,207,510 B1), Cunningham (USP: 6,177,703 B1), Eitan (USP: 5,966,603), and Yamamoto et al. (USP: 5,381,756) are cited as of interest.

4. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Art Unit: 2818

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (703) 305-0089. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910. The Fax number for the organization where this application or proceeding is assigned is (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

AL

AH

  
HOAI HO  
PRIMARY EXAMINER